REMARKS

Claims 1 - 20 remain active in this application. Claims 12 - 20 have been withdrawn from consideration as being non-elected, without traverse, in response to a requirement for restriction. Claims 1, 2, 9 and 11 have been amended to correct grammatical errors and to emphasize novel aspects of the invention as originally claimed. No new matter has been introduced into the application.

The specification has been amended in several locations to correct spelling and grammatical errors. An erroneous reference number has been deleted from Figure 1. No new matter has been introduced into the application.

Claims 1, 8, 9 and 11 have been rejected under 35 U.S.C. §102 as being anticipated by Kumagai et al. Claims 1 – 11 have been rejected under 35 U.S.C. §102 as being anticipated by Huang et al. Claims 1 – 11 have been rejected under 35 U.S.C. §102 as being anticipated by Chidambarrao et al. These rejections are respectfully traversed in view of the remarks below.

The present invention discloses a method of enhancing carrier mobility for different transistor types on a common chip. As recited in claim 1, the method is comprised, in sequence, of: (1) providing a first layer of material providing a first stress level is applied on a surface of the chip; (2) selectively reducing said first stress level of a portion of said first layer of material; (3) providing a second layer of material providing a second stress level on a surface of the chip; and (4) selectively reducing said second stress level of a portion of said second layer of material. Conversely, Kumagai is directed to alteration of carrier mobility and provides twelve embodiments in which adjustment of carrier mobility is achieved to some degree by different structures formed by different methods. However, none of these twelve embodiments answers the method claimed.

Specifically, the Examiner contends that the stress control film (191) in Kumagai somehow anticipates a dual-layered method as disclosed in claim 1 of the present invention because it "does not require the first layer of material [to be] different from the second layer of material" (see page 4 of the Office Action). However, it should be noted at the outset that Kumagai does not teach the use of layers other than for grain size control in the fifth

embodiment; therefore, the 35 U.S.C. §102 rejection is incorrect on its face. While Kumagai may teach some of the steps recited in claim 1 in different, respective embodiments, it does not teach or suggest a combination of the steps as recited in claim 1, or the steps can be changed. In other words, Kumagai does not teach nor suggest the four steps in combination, much less in sequence, as recited in claim 1 as amended. Therefore, Kumagai does not, in fact, answer the explicit recitations of claim 1, nor the dependent claims 2-11, and thus does not anticipate any claim in the application.

Furthermore, the Examiner does not take into account the recitation that a first stress level is to be applied by the first layer, and a second stress level is to be applied by the second layer. Kumagai also does not teach nor suggest the importance of applying different stresses to different layers. Furthermore, the second layer is applied by a different process and/or with different process parameters (see page 14 of the specification of the present invention). Kumagai does not teach (or suggest) reducing of stresses in stressed layers after formation thereof.

With regard to the Huang and Chidambarrao references, the Examiner contends that both references anticipate the claimed invention. However, the Examiner acknowledges that Huang and Chidambarrao teaches the selective removing of the first layer portion covering one of the transistors, thereby leaving the NMOS or NFET exposed (see pages 5 and 6 of the Office Action; see paragraph 30 and Figure 2 in Huang; see paragraph 28 and Figures 4a – 4b in Chidambarrao). The present invention, as recited in claim 1, does not rely on the removing of any portion of the first layer. Rather, claim 1 of the present invention teaches the reducing of the first stress level of a portion of the first or second layer which remains in place. To completely remove the first layer from the NMOS portion of the chip would defeat the purpose of the invention. Specifically, the first layer facilitates the formation of openings for connections to the source, drain and gate of the transistors while avoiding damage thereto (see pages 11-12 in the specification). Therefore, neither Huang nor Chidambarrao answers the explicit recitations of claim 1, nor the subject matter of dependent claims 2-11, and thus does not anticipate any claim in the application.

Further, the nonstatutory double patenting rejection is now moot in view of the above

remarks. Specifically, since the Chidambarrao reference teaches the removal of the "first spacer material", while the present invention teaches the reduction of the first level stress level of a portion of the first layer, the inventions are completely different. Therefore, a terminal disclaimer is not warranted in the present invention as its method disclosed therein is completely different from the Chidambarrao reference.

Accordingly, it is respectfully submitted that the rejection of claims 1 - 11 for anticipation by Kumagai, Huang or Chidambarrao is clearly in error and untenable. Therefore, reconsideration and withdrawal of the rejection under 35 U.S.C. §102 of claims 1 – 11, along with the nonstatutory double patenting rejection of claim 1, and the allowance of the application are respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0458 (International Business Machines Corporation – Fishkill).

Respectfully submitted,

Marshall M. Curtis
Reg. No. 33,138

Whitham, Curtis & Christofferson, P. C.
11491 Sunset Hills Road, Suite 340
Reston, Virginia 20190

(703) 787-9400
Customer Number: **30743**

In the drawings:

Please approve the deletion of reference "24" in Figure 1, as shown in red on the marked-up copies (Annotated Marked-Up Drawings), and substitute therefore the attached Replacement sheet of Figure 1 which implements the change.

Annotated Marked-Up Drawings

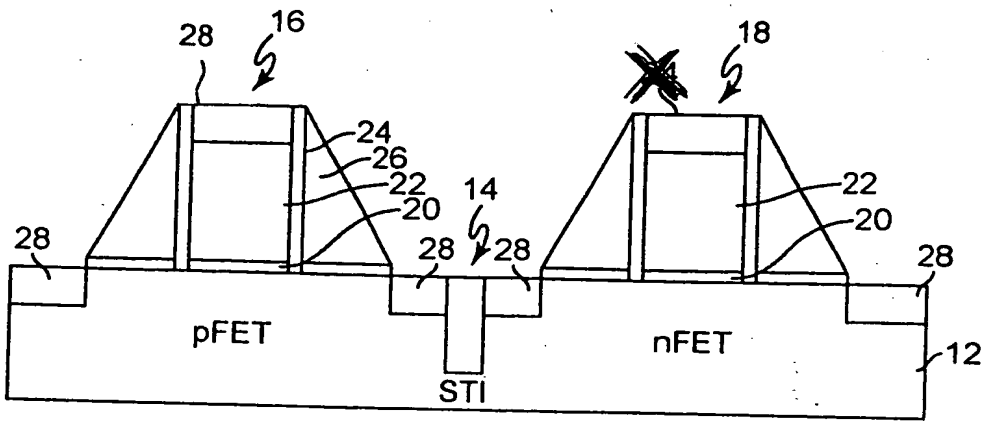

FIGURE 1

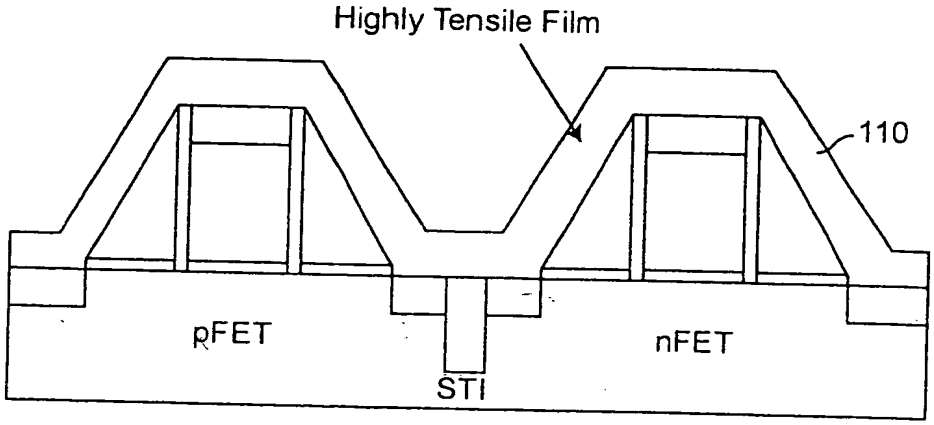

FIGURE 2

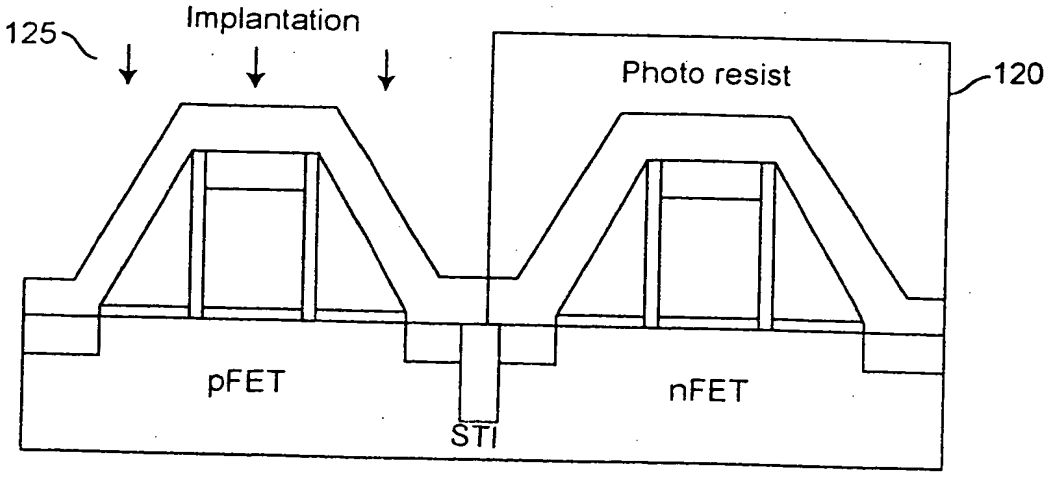

FIGURE 3